Figure 3 shows the structure of a prior art error correction device.

Figure 4 shows the procedure (flow chart) of the processing of the prior art error correction device.

Figure 5 shows the structure (block diagram) of the error correction device of Embodiment 1 of the present invention.

Figure 6 shows the procedure of the processing of the error correction device.

Figure 7 shows the structure of the error correction device of Embodiment 2 of the present invention.

Figure 8 show the procedure of the processing of the error correction device.

Figure 9 shows the structure of the error correction device of Embodiment 3 of the present invention.

Figure 10 shows the procedure of the processing of the error correction device.

Figure 11 shows the structure of the error correction device of Embodiment 4 of the present invention.

Figure 12 shows the structure of the error correction device of Embodiment 5 of the present invention.

Figure 13 explains the error-containing codes and the data transfer range of the error correction device of the embodiment.

Figure 14 shows the procedure of the processing of the error correction device.

Figure 15 shows the structure of the error correction device of Embodiment 6 of the present invention.

Figure 16 is a timing chart illustrating the operation of the error correction device of the embodiment

Figure 17 explains the error-containing codes and the data transfer range of the error correction device of the embodiment.

Figure 18 shows the structure of the error correction device of Embodiment 7 of the present invention.

Figure 19 conceptually shows the effects of the pipeline processing in the error correction device of the embodiment.

Figure 20 shows the structure of the error correction device of Embodiment 8 of the present invention.

Figures 21A and 21B conceptually show the reference tables stored and managed by the control unit in the error correction device of the embodiment in order to facilitate pipeline processing.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will be described as follows based on its embodiments.

(Embodiment 1)

The present embodiment differs from the prior art in that a mid-term result register is provided and that an error-containing code detection signal and an error-containing code word signal are entered to the system control unit from the syndrome calculator.

Figure 5 shows the structure of the error correction device of the present embodiment. In the device, the system control unit 1, the DMA control unit 2, the bus control unit 3, the buffer memory 4, the syndrome

calculator 5, the error corrector 6, and the error detector 7, which are basically identical to the components in the prior art, are referred to with the same reference numbers. (In the present and the following embodiments, the identical components are referred to with the same reference numbers unless they must be distinguished. This holds true for signals).

The same as in the prior art device, the bus control device 3, the buffer memory 4, the syndrome calculator 5, the error corrector 6, and the error detector 7 are connected via the data bus 11.

The DMA command 12, the DMA request 13, the buffer memory access signal 14, the syndrome supply signal 15, the syndrome 16, the access request signal 17, the error corrector access signal 18, the correction completion signal 19, the error detector data supply signal 20, and the error detection signal 21 are also basically identical to those in the prior art device, so they are referred to with the same reference numbers.

The mid-term result register 8, which is connected with the error detector 7, stores the mid-term results of the error detecting process done in the error detector 7. The error-containing code detection signal 22, which indicates that an error-containing code word has been detected by the syndrome calculator 5, is transmitted to the system control unit 1 and to the error detector 7. The error-containing code word signal 23, which indicates in which code word the error is detected by the syndrome calculator 5, is transmitted to the system control unit 1.

The behavior of the error correction device thus structured will be described as follows, with reference to Figure 6.